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Studies on the physical properties of the thin-film metal/$PtSe_2$ interfaces

Summary for general public

Development of the conventional silicon (Si)-based electronics is reaching technological limitations. Further progress in the electronic technology requires integration of new materials into existing Complementary Metal-Oxide Semiconductor (CMOS) technology. The integrated materials, used in selected elements allow to increase their functionality and further miniaturization. Two-dimensional (2D) materials are a potential candidate for use in active layers of such elements. These materials have limited electrons movement to the two-dimensional (2D), nanometric thick layer. This feature causes anisotropy of the material's physical properties in the layer in comparison to the direction perpendicular to it. One of these properties is the electrical conductivity. Within the layer obtained the charge carriers mobility is comparable to ideal three-dimensional (3D) high-mobility crystals with the thickness 1000 times larger, while in the perpendicular direction it is several orders of magnitude lower. The best example is graphene (Gr) layer containing the single carbon atoms layer. This layer allows for flow current density value which is unimaginable for conventional electronics materials. Availability and relatively simple to fabrication Gr layer, allowed to made it dominate 2D material for several years. However, the aging effects and destructive water vapor adsorption in the atmospheric air are causing scientists to be interested in other types of the layered materials. These types of materials include e.g.: topological insulators (TI) or Transition Metal Dichalcogenides (TMDs), which contain 5 and 3 atomic layers in the elemental layer structure, respectively. These materials properties still requires a number of basic studies, including interaction with metallic layers, without which it is impossible to fully understand and apply them later. Physical properties determination under micrometric scale allows for its understanding the systems also on a larger scale.

The research works planned in the project are focused on recently synthesized TMDs (in particular $PtSe_2$) materials. They exhibit in theory physical properties (e.g. high charge carriers mobility and concentration), slightly smaller than Gr. In contrast to Gr, $PtSe_2$ surface shows much better long-term stability during air exposition. An additional advantage of the examined material is the dependence of the electronic structure and nature of conductivity on the layers number (thickness) in the conductivity channel. This phenomena allows to creation of various types of elementary electronic devices using one type of material in the active layer. The possibility of modifying the electronic properties of the active layer by its thickness, still remaining in the range of several nanometers, will open wide application possibilities in the future, even compared to Gr layers. However, basic research should solve the emerging challenges in the case, such as problematic creation of low-resistance metallic contact by means of metallic layers deposition using physical methods followed by lithography process. This challenge is caused by the low chemical activity of the substrate and the need to apply edge ohmic contact architecture.

The main research problem of the proposed project is focused on the electrical and global morphology characterization of the transition metal/2D materials surfaces, in particular $PtSe_2$ junctions. This issue is not fully understood and properties of the transition metal/$PtSe_2$ junctions are an important elements of basic knowledge. The main proposal's objectives are: analyses of the properties of the transition metals/$PtSe_2$ interfaces, determination of the post-deposition temperature treatments on the junctions resistivity and characterization of metallic contacts containing a buffer layer made of analyzed metals on a micrometric scale. The final results of this work will allow to control the junction properties, which will potentially useful to the construction of devices prototypes containing a thin layer of $PtSe_2$ as the active element.

Recent experimental works, carried out by the author of the project, showed the significant influence of the buffer layer on the electrical contact properties and the Gr - metal interface. It was shown that metallic layer grow and the associated interdiffusion between the metal, and the substrate are determined by the presence of layered material (Gr) on the interface in the system. In addition, surface structurization was also carried out to determine the physical properties of the layer and junctions the Gr-based systems on the insulating substrate (SiC). Until now, the focus has been on creating electrical contact with the required minimum connector resistance, however, this process can be significantly optimized by: material selection, growth parameters, and ohmic contact architecture, which seems to be crucial for the materials under consideration, especially for $PtSe_2$ layer.