The development of microelectronics is driven by expectations of the users to improve electronic equipment functionality on one hand, and the miniaturization, reduction of cost and power consumption of integrated circuits on the other. The beneficiary of the evolution of semiconductor technology is digital block design. By reducing transistor size, digital blocks become smaller, faster and more energy efficient. The progressive miniaturization and the need to reduce the supply voltage imply the difficulties in design of analog circuits associated with the continuous decrease of voltage range to encode signals that carry information. Therefore, the implementation of circuits realized the analog signal processing in a voltage is becoming significantly more and more difficult.
A new method of analog circuit design based on encoding voltage signals in a form of time intervals (TMSP - *Time-Mode Signal Processing*) has emerged. One of the key components of the TMSP system is a time-to-digital converter (TDCs - *Time-to-Digital Converter*) that converts the time intervals into a digital representation. The most famous application of the TDC is the all-digital phase locked loop (ADPLL). The ADPLL was invented a decade ago and is used in majority of produced today's mobile phones.

The research objective is to design and implement in a deep submicron CMOS process a metastability-insensitive successive approximation time-to-digital converter (MI SA-TDC) with an architecture optimized in terms of performance, design complexity, energy consumption, conversion time, and die area. The important advantage of the SA-TDC is a small number of blocks required to build this converter (e.g. in the SA-TDC can be used only a single time comparator in contrast to 256 time comparators needed in the popular 8-bit TDC based on Vernier principle). In order to achieve a high accuracy of the SA-TDC, the unit delay corresponds to the propagation time of signal through the logic gate (e.g., an inverter).
The principle of the SA-TDC is based on successive delaying two events defining the start and the stop of input time interval by the use of binary-scaled delays. In each conversion step, the event which arrives earlier is delayed by the corresponding latency, so that both events are at the end of the conversion closer in time than the unit delay (*LSB*). The time-to-digital conversion based on successive approximation can be similar to evaluation of the unknown mass by the use of a pan balance with a set of binary-scaled weights. The operation principle based on systematically adding a new weight to this pan, which currently accumulates less mass. If weight was placed in the pan with unknown mass, then the corresponding output bit of digital code word equals ‘0’. Otherwise, the bit is evaluated to ‘1’.
In the proposed SA-TDC architecture with two feedback loops, both events are delayed in separate delay loops using binary-scaled delay components. After using each delay component, both events are compared by time comparator in order to identify which event is earlier. This operation may be relatively ‘long’ because the time comparator may spend a long time on distinguishing the chronology of events that arrive almost simultaneously. Therefore, to ensure the correct time-to-digital conversion, it is necessary to introduce an additional delay in each loop in order to get an extra time for the time comparator to recognize which event came first.

In scientific literature, the metastability is indicated as one of the fundamental problems of conversion time intervals based on successive approximation. The metastable states imply an uncontrolled increase of decision-making time at comparator outputs when the both events arrive quasi-simultaneously. In the SA-TDC, the metastable states are the source of gross errors and cause getting a completely wrong conversion result. The proposed SA-TDC will be equipped with the anti-metastability mechanism. The proposed method of anti-metastability mechanism is simple and can be adopted to other types of TDC.