The aim of this project is the exploration and realization of a new concept of massively parallel time-to-digital converters (TDC) that are realized in a nanometer-scale CMOS process technology and are optimized for time-of-flight (ToF)-based matrix of pixel detectors.

The TDCs are used to digitize the detected time-of-arrival of a photon (e.g., X-ray, infrared) or a particle, while denoting the detector's position within the matrix (i.e., spatiotemporal detection). Given a large number (thousands or even millions in the future) of intended pixels to be supported, each pixel detector is envisioned to be served by a dedicated TDC. This will maximally increase the detection speed/rate while keeping its detection unavailability (i.e., "dead time") to a minimum. The key TDC parameters are: fine picosecond-level resolution, small area and low power consumption; hence, they are best implemented in nanometer-scale (nanoscale) CMOS process technology. Unfortunately, this process choice makes it incompatible with the photon/particle detectors, whose key parameters are the quantum and detection efficiencies in the intended spectrum range, which rarely agrees with that of silicon.

The hybrid detector thus attempts to solve this technology mismatch problem by stacking the pixel detector die on top of the CMOS silicon die of TDC matrix, while interconnecting them with tiny bump bondings. In this arrangement, the TDC dimensions must naturally be lower than the pitch of pixel detectors, which is now typically around 50-100 μm but expected to continue shrinking in the future.

Time-of-flight (ToF) measurements are becoming essential to the advancement of detectors for positron emission tomography (PET), high-energy physics, 3D vision, ultra-high-resolution microscopy, near-infrared imaging, tie resolved Raman spectroscopy, quantum security, and many others. In many of these applications, a real-time millimeter-level timing resolution along the direct line of response is required.

The authors of this proposal aim to publish the resulting research outcome in prestigious international IEEE conferences, as well as prestigious journal publications (JCR list). Furthermore, this research will bring important answers to the main questions raised in the wide field of microelectronics regarding the design and implementations of fast mixed-signal integrated circuits. The new solutions and methods worked out during this project will have a great deal of universal value and applicability, so they are expected to be used in other applications, especially where it is important to swiftly process precise timing signals while maintaining low power consumption.