Popularnonaukowe streszczenie projektu (ang)

Within the project the proposer plans to conduct a comprehensive experimental studies to determine key parameters of 2D electron gas (2DEG) formed at surfaces and interfaces of III-V semiconductors. The studies will be carried out for model systems of III-V semiconductors with narrow band-gap, prepared intentionally to contain 2DEG. Proposed research will include: the 2DEG band-structure mapping, estimation of the magnitude of many-body interactions in 2DEG, as well as influence of the system disorder on the 2DEG parameters. The experiments will be carried out on samples of III-V compound semiconductor crystals (e.g InAs, InSb). These surfaces will be adsorbed with molecules of chalcogens in order to generate an electrical charge on the surfaces and cause a band-bending necessary for 2DEG to form. In general the studied surfaces will be three component systems and a large number of metastable ordered surface phases are expected to exist, each one leading to characteristic band bending at the surface. The main studies will be done using the most efficient and straightforward method allowing for the band-structure mapping including many-electron and electron phonon effects as well as effects of scattering, that is, angle resolved photoelectron spectroscopy (ARPES). Investigations are planned for different surface crystallographic orientations and for different surface stoichiometries. The planned investigations will be carried out in the context of emerging application of similar physical systems in devices of mainstream digital electronics. For the technology the most important is the system with 2DEG induced by external electric field the source of which is a biased gate. Such system is absolutely crucial for contemporary digital electronics. To a large extent it decides about the switching speed of the logic networks (i.e. about functional speed of digital processors and memory). In the present situation, when the concept of miniaturization in electronic is essentially exhausted, further development will be possible through increasing of the carrier mobility in FET conducting channel. Many facts indicate now that the 2DEG on III-V's will be the „workhorse" of future digital electronic. However, contemporary literature of the topic does not answer such questions as: what factors limit the mobility of electrons in 2 DEG based on |III-V materials? To what extent it is possible to realize theoretical possibility of 50-fold increase of switching speed of logic networks after substituting silicon in the n-FET channel with III-V's?

Proposed investigations are aimed also for providing the robust data needed for estimating practical switching speed limits of logic electronic designed based on 2DEG on III-V semiconductors. devices.